UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,010	10/02/2003	Consuelo N. Tangpuz	11948.26	9241

27966 7590 01/10/2005

KENNETH E. HORTON
KIRTON & MCCONKLE
60 EAST SOUTH TEMPLE
SUITE 1800
SALTLAKE CITY, UT 84111

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,010	TANGPUZ ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *1-23 and 34-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 02/17/2004 is acceptable.

Election/ Restriction

2. Applicant's election with traverse of Invention II, **claims 24-33**, in the reply filed on 12/06/2004 is acknowledged. The traversal is on the ground(s) that the process as recited in the invention of claim 24 of Invention II is not different than the proposed process, as cited by the examiner in the restriction requirement as an example, to form the device of Invention I. This is true, however, unpersuasive because the difference between Invention I and II, as cited by the examiner, is not in the process of the invention of claim 24 of Invention II, but in the process of the invention of claim 32 of Invention II. And since the invention of claim 24, being a linking claim, of Invention II is not found allowable, the claims of Invention I are withdrawn from consideration, as detailed below.

The requirement is still deemed proper and is therefore made FINAL.

3. **Claims 1-23 and 34-39** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 12/06/2004, as detailed above.

Specification

4. The disclosure is objected to because of the following informalities:

- Page 11, last line of paragraph [0048], misspelled "miroinches"
- Page 11, paragraph [0048], line 2, mistyped "6" in "as shown in Figure 6", which should be changed to "as shown in Figures 5 and 7" because the description following the phrase is clearly for Figures 5 and 7.

Appropriate correction is required.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: lead structure 22 (paragraph [0031]). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 24, 27, and 33** are rejected under 35 U.S.C. 102(e) as being anticipated by Hwee et al. U.S. Patent 6,510,976 (the '976 patent).

The '976 patent discloses in Figures 1-5 and respective portions of the specification a method for forming a semiconductor package as claimed.

Referring to **claim 24**, Hwee discloses in Figs. 1 and 3A-3E a method for forming a semiconductor package, the method comprising:

providing a die (320) with a metal stud (325, "such as copper posts", column 5, lines 23-24) on a bond pad;

providing a leadframe (100) containing a plurality of leads, the leadframe containing a solderable area (340, Fig. 3D and column 5, last paragraph) surrounded by a solder dam (355, Fig. 3E and column 6, lines 22-30);

providing a solder paste (column 6, lines 17-20: "during reflow ...the solder balls 330 change to a molten state") in or on the solderable area;

attaching the die and the leadframe; and

molding a molding material (Fig. 4, step 445) around a portion of the die and a portion of the leadframe.

Referring to **claim 27**, although not explicitly disclosed, attaching the die to the leadframe is by flipping the die (320) and contacting the metal stud (325) with the solder paste (330), as is suggested by the name Flip-Chip (Title).

Referring to **claim 33**, as detailed above, Hwee discloses re-flowing the solder paste after attaching the die and the leadframe.

Claim Rejections § 102 & § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 25-26** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the '976 patent.

The '976 patent discloses a method for forming a semiconductor package as claimed and as detailed above for claim 24, including the metal stud 325 formed of copper but fails to teach that the copper stud contains substantially no Pb, and further fails to teach that the amount of Pb in the copper stud is less than about 1 ppm. However, since the '976 patent is completely silent about the Pb component for the copper stud, it is reasonable to conclude that the copper stud contains substantially no Pb or the amount of Pb in the copper stud is less than about 1 ppm. In

addition, there has been a tendency in the art not to use Pb or Pb-related materials. See also, as an example, U.S. Patent Application Publication 2003/0089923 by Oida et al. which discloses in general the impact of, and thus the requirement for manufactures to reduce, Pb (lead) in the environment (BACKGROUND OF THE INVENTION), and U.S. Patent 6,457,233 to Shimizu which also discuss the impact of Pb in the environment (column 1, lines 50-55) and which further discloses that 1 ppm Pb or below is a concentration value one would use to indicate the insignificant presence of Pb (column 4, first full paragraph).

Claim Rejections - 35 USC § 103

8. **Claims 28-30** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '976 patent in view of Venkateshwaran et al. U.S. Patent 6,316,822 and further in view of Litani et al. U.S. Patent Application Publication 2004/0169261.

Referring to **claim 28**, the '976 patent discloses a method for forming a semiconductor package substantially as claimed and as detailed above for claim 24, including the solderable area 340 on which the solder paste 330 is located, but fails to disclose that the solderable area is supplied with a pad containing a non-oxidizable noble metal.

Venkateshwaran on the other hand, in disclosing a semiconductor package including a leadframe 12 and IC dies 11a, 15a including a bonding pad (Fig. 1), teaches that to insure reliable attachment of the solder to the leads of the leadframe as well as to the bonding pad (chip contact pads), a layer of a noble metal is deposited over the base metal of the leadframe (column 7, first paragraph). Litani, in also disclosing a semiconductor package including a copper leadframe (paragraph [0024]) and a die including a bonding pad, teaches that by plating a noble

metal (palladium) *only* to a bonding pad ("necessary portions") of the leadframe where bonding is to occur (paragraph [0006]), a much cheaper leadframe can be provided (paragraph [0009]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the solderable area of the '976 patent with a pad containing a non-oxidizable noble metal. One would have been motivated to make such a modification in view of the technical teachings in Venkateshwaran that a noble metal deposited over the base metal of the leadframe insures reliable attachment of the solder to the leads of the leadframe as well as to the chip contact pads and further in view of the economic teachings in Litani that plating a noble metal *only* to a bonding pad of the leadframe helps producing a less expensive leadframe.

Referring to **claims 29 and 30**, the solder dam 355 of the '976 patent's leadframe thus modified further includes a metal oxide (column 6, lines 22-28), meeting the requirement of the Markush group, and wherein the metal oxide is provided by providing a metal and then oxidizing the metal (paragraph bridging columns 4 and 5).

9. **Claim 32 is** rejected under 35 U.S.C. §103(a) as being unpatentable over the '976 patent in view of Siegel et al. U.S. Patent Application Publication 2003/0143406.

The '976 patent discloses a method for forming a semiconductor package substantially as claimed and as detailed above for claim 24, including the step 245 for molding a molding material around a portion of the die and a portion of the leadframe but fails to disclose that the molding includes a film assisted molding process.

Siegel, in disclosing a system and method for a molding process for an integrated circuit, teaches in paragraph [0005] that a first type of film assisted molding process includes a

compliant material for cushioning the clamping action of the transfer mold, which is inherent for a molding process, against the IC die surface.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '976 patent's device using a film assisted molding process. One would have been motivated to make such a modification in view of the teachings in Siegel that a film assisted molding process helps cushioning the clamping action of the transfer mold against the IC die surface.

10. **Claim 24 is** rejected under 35 U.S.C. §103(a) as being unpatentable over Lo et al. U.S. Patent 6,507,120 (the '120 patent) in view of Melton U.S. Patent 5,316,205.

The '120 patent discloses a method for forming a semiconductor package substantially as claimed but fails to disclose providing a solder paste for a solderable area. In particular, the '120 patent discloses a method for forming a semiconductor package, the method comprising:

providing a die (210, Fig. 6) with a metal stud (218, "bumps" formed of a material such as gold, column 3, lines 12-15) on a bond pad (216) (and note that "stud" is interpreted as A small knob, nail head, or rivet fixed in and slightly projecting from a surface[1] as specific geometry for the claimed stud is not given in the specification);

providing a leadframe (defined by a plurality of leads 202, column 3, lines 4-5) containing a plurality of leads (202), the leadframe containing a solderable area (generally

---

[1] *The American Heritage® Dictionary of the English Language, Third Edition* copyright © 1992 by Houghton Mifflin Company. Electronic version licensed from InfoSoft International, Inc. All rights reserved.

defined by opening 222) surrounded by a solder dam ("solder mask" 220, column 3, lines 30-35);

attaching the die and the leadframe; and

molding a molding material (226) around a portion of the die and a portion of the leadframe.

However, the reference fails to disclose providing a solder paste in or on the solderable area.

Melton, in disclosing a method for forming a gold bump (112, Fig. 3) connection to bond pad 120 using a solder paste (122), teaches that after the heating an reflow process, the molten solder paste helps bonding the gold bump to the bond pad (column 4, lines 12-53).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '120 patent's gold stud 218 with a solder paste in or on the solderable area of the lead 202. One would have been motivated to make such a modification in view of the teachings by Melton that a solder paste helps bonding the gold bump to the lead.

11. **Claims 28-29 and 31** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '120 patent in view of Melton as applied to claim 24 and as detailed above and further in view of Venkateshwaran et al. U.S. Patent 6,316,822 and further in view of Litani et al. U.S. Patent Application Publication 2004/0169261.

Referring to **claim 28**, the '120 patent discloses a method for forming a semiconductor package substantially as claimed and as detailed above for claim 24, including the solderable area 222 on which a solder paste, such as solder paste 122 taught by Melton as detailed above, is

located, but fails to disclose that the solderable area is supplied with a pad containing a non-oxidizable noble metal.

Venkateshwaran on the other hand, in disclosing a semiconductor package including a leadframe 12 and IC dies 11a, 15a including a bonding pad (Fig. 1), teaches that to insure reliable attachment of the solder to the leads of the leadframe as well as to the bonding pad (chip contact pads), a layer of a noble metal is deposited over the base metal of the leadframe (column 7, first paragraph). Litani, in also disclosing a semiconductor package including a copper leadframe (paragraph [0024]) and a die including a bonding pad, teaches that by plating a noble metal (palladium) *only* to a bonding pad ("necessary portions") of the leadframe where bonding is to occur (paragraph [0006]), a much cheaper leadframe can be provided (paragraph [0009]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the solderable area of the '120 patent with a pad containing a non-oxidizable noble metal. One would have been motivated to make such a modification in view of the technical teachings in Venkateshwaran that a noble metal deposited over the base metal of the leadframe insures reliable attachment of the solder to the leads of the leadframe as well as to the chip contact pads and further in view of the economic teachings in Litani that plating a noble metal *only* to a bonding pad of the leadframe helps producing a less expensive leadframe.

Referring to **claims 29 and 31**, the solder dam 220 of the '120 patent's leadframe thus modified further includes a polymer material ("thermoset solder mask", column 3, lines 30-31), meeting the requirement of the claimed Markush group, and wherein the polymeric material is provided by screen printing (column 3, lines 31-34).

12. **Claim 24 and 33** are rejected under 35 U.S.C. §103(a) as being unpatentable over Pu U.S. Patent Application Publication 2002/0182843 (the '843 publication) in view of the '120 patent.

The '843 publication discloses a method for forming a semiconductor package substantially as claimed but fails to disclose providing a solder dam around a solderable area. In particular, the '843 publication discloses a method for forming a semiconductor package, the method comprising:

providing a die (2, Fig. 6) with a metal stud (chip bump 3, with "stud" is interpreted broadly) on a bond pad (not shown);

providing a leadframe (7) containing a plurality of leads (only one is shown), the leadframe containing a solderable area (generally defined by a contact area between bump 3 and lead 7);

providing a solder paste (which is also bump 3) in or on the solderable area;

attaching the die and the leadframe; and

molding a molding material (paragraph [0009]) around a portion of the die and a portion of the leadframe.

However, the reference fails to disclose that the solderable area is surrounded by a solder dam.

The '120 patent, in disclosing a process of forming substantially similar to that of the '843 publication and that of the invention – as detailed above, teaches that in order to ensure the yield of the process of forming, it is preferred that the first surface 204 of leads 202 is covered by a solder dam (solder resistance, or solder mask, column 3, lines 24-37).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '843 publication's solderable area such that it is surrounded by a solder dam. One would have been motivated to make such a modification in view of the teachings by the '120 patent that that a solder dam increase yield of the method of forming the semiconductor package. It is noted that although the '843 publication appears to teach away with the use of a complicated solder dam, the issue here, nevertheless, is the question of obviousness to one of ordinary skill in the art, and it would certainly appear to be so because the change results in an added improvement to the '843 publication's process.

Referring to **claim 33**, the '843 publication further disclose re-flowing the solder paste after attaching the die and the leadframe (paragraph [0024]).

13. **Claims 25-26 and 28** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '843 publication in view of the '120 patent as applied to claim 24 and as detailed above and further in view of Shimizu U.S. Patent 6,457,233.

The '843 publication discloses a method for forming a semiconductor package substantially as claimed and as detailed above for claim 24, including the metal stud 3 and the solderable area, but fails to disclose that the stud contains substantially no Pb as recited in claim 25, and further fails to teach that the amount of Pb in the stud is less than about 1 ppm as recited in claim 26. The publication further fails to disclose that the solderable area contains a pad containing a non-oxidizable metal as recited in claim 28.

Shimizu, in disclosing a method for forming a semiconductor package, discuss the impact of Pb in the environment in the occurrence of the so-called soft errors (column 1, lines 50-55)

and which further discloses that 1 ppm Pb or below is a concentration value one would use to indicate the insignificant presence of Pb (column 4, first full paragraph), thereby teaching that conductive studs should not contain Pb. To be more specific, Shimizu teaches in Fig. 1 two multilayered studs jointed together by a solder paste, all of which are Pb free and containing a few sub-layers of non-oxidizable metals (Ti, Au,...).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '843 publication's stud such that it contains substantially no Pb, that the amount of Pb in the stud is less than about 1 ppm, and that the solderable area contains a pad containing a non-oxidizable metal. One would have been motivated to make such a modification in view of the teachings in Shimizu that such a structure is environmental friendly and helps reduce soft errors.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
January 03, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800